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Dickerson

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[54] METHOD AND CIRCUIT FOR PROCESSING AND FILTERING SIGNALS

[75] Inventor: Roger W. Dickerson, Loveland, Ohio

[73] Assignee: Xetron Corporation, Cincinatti, Ohio

[*] Notice: The portion of the term of this patent subsequent to Nov. 16, 2010 has been disclaimed.

[21] Appl. No.: 134,807

[22] Filed: Oct. 12, 1993

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 806,058, Dec. 11, 1991, Pat. No. 5,263,191.

[51] Int. Cl.^{6} H04B 1/10

[52] U.S. Cl. 455/304; 455/65; 375/346; 327/311; 327/317; 327/361

[58] Field of Search .... 375/102, 104, 99, 100, 375/11–15; 328/162, 165, 164; 360/38.1; 358/314; 329/320; 455/295, 296, 65, 304; 307/556, 542; 364/724.19, 724.2; 333/18, 28 R

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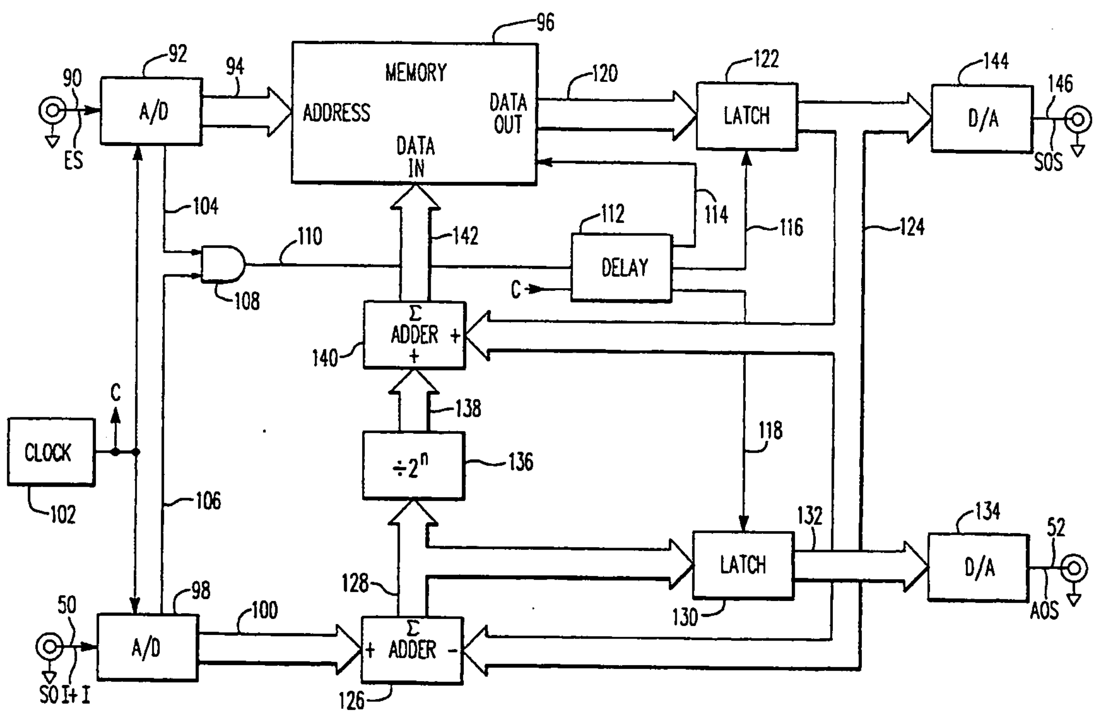
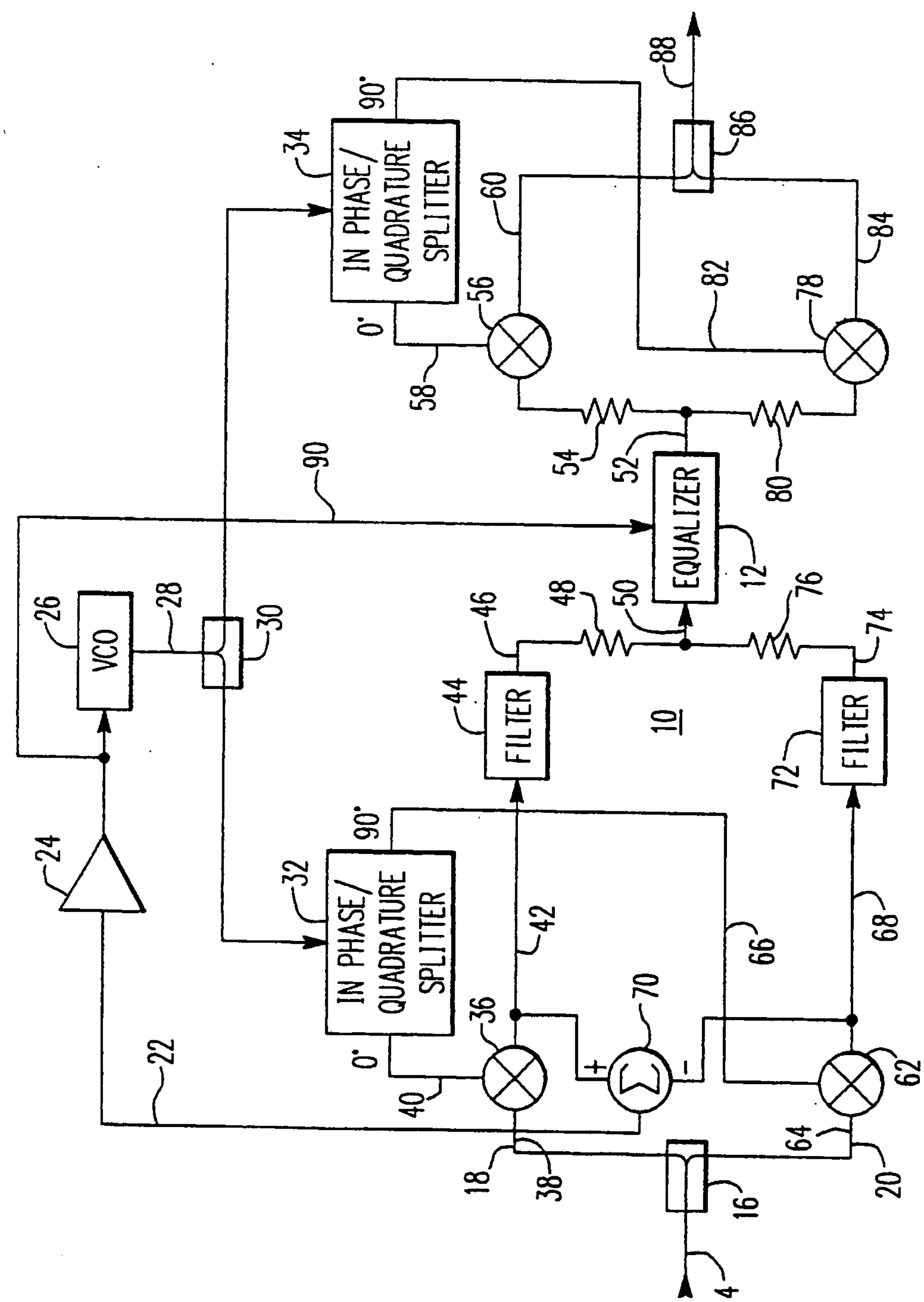
Primary Examiner—Edward F. Urban
Assistant Examiner—Mark D. Wisler

[57] ABSTRACT

A method for processing electrical signals includes the steps of: storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal in a memory; selecting one of the first data signals in response to a second input signal; combining the selected one of the first data signals with a second data signal representative of a subsequent instantaneous amplitude of the first input signal, to produce a difference signal; producing a first output signal in response to the difference signal; and combining the difference signal and the selected first data signal to produce a modified data signal and for replacing the selected one of the first data signals with the modified data signal in the memory. The method can be performed by an equalizer in a circuit for compensating for amplitude variations in a radio frequency signal or by a comb notch filter. The invention also encompasses circuits and combinations of such circuits which perform the above signal processing method.

23 Claims, 7 Drawing Sheets




VCO
IN PHASE/ QUADRATURE SPLITTER
IN PHASE/ QUADRATURE SPLITTER
FILTER
FILTER
EQUALIZER
0°
90°
0°
90°
10
12
14
16
18
20
22
24
26
28
30
32
34
36
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42
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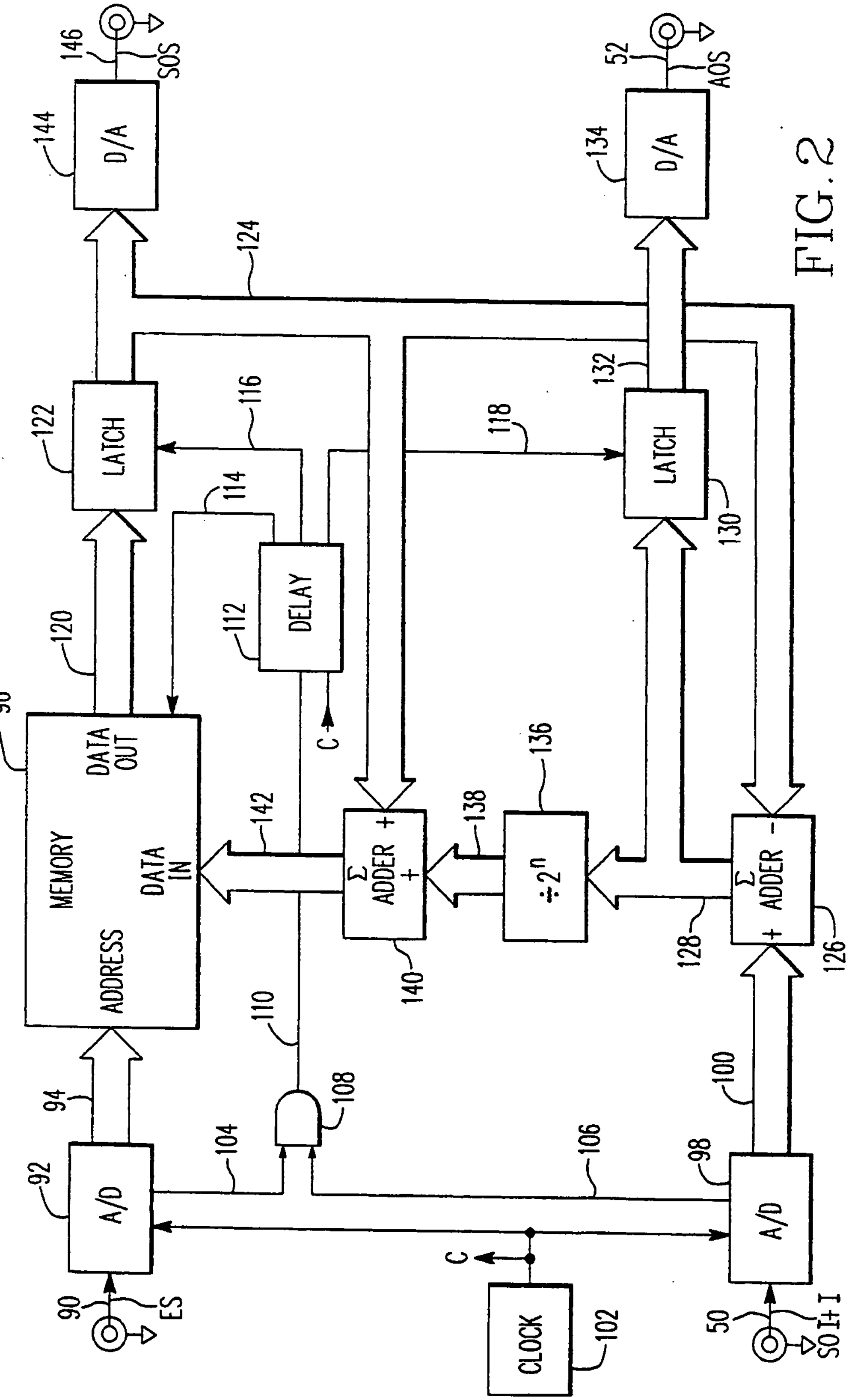
90

FIG. 1



A/D
MEMORY
ADDRESS
DATA IN
DATA OUT
LATCH
DELAY
D/A
Σ ADDER
÷2ⁿ
CLOCK
ES
SOI+I
SOS
AOS
C
90
92
94
96
98
100
102
104
106
108
110
112
114
116
118
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142
144
146
50
52

FIG. 2

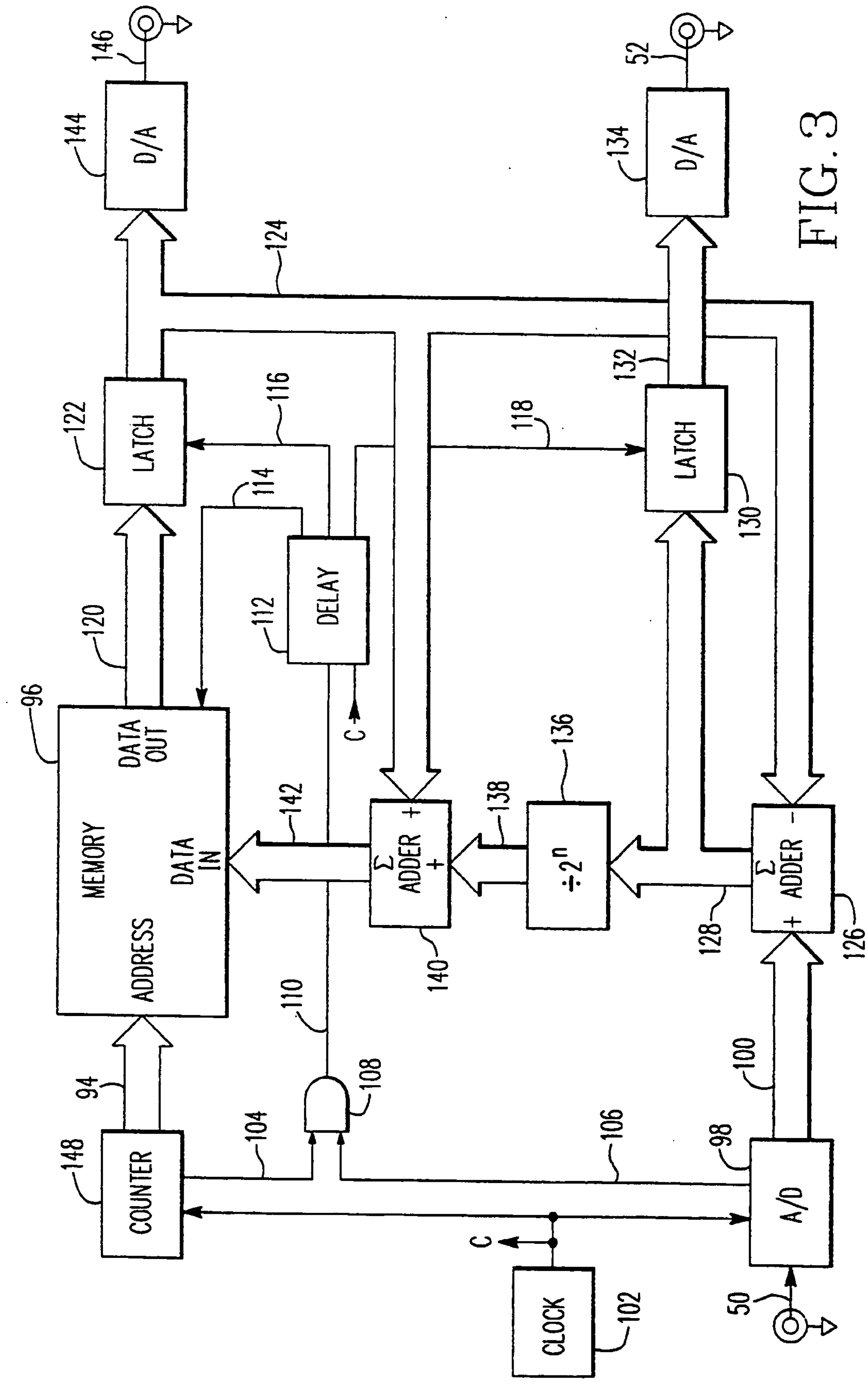

D/A
D/A
LATCH
LATCH
DELAY
MEMORY
DATA OUT
DATA IN
ADDRESS
Σ ADDER
÷2ⁿ
Σ ADDER
COUNTER
CLOCK
A/D
C
C

FIG. 3

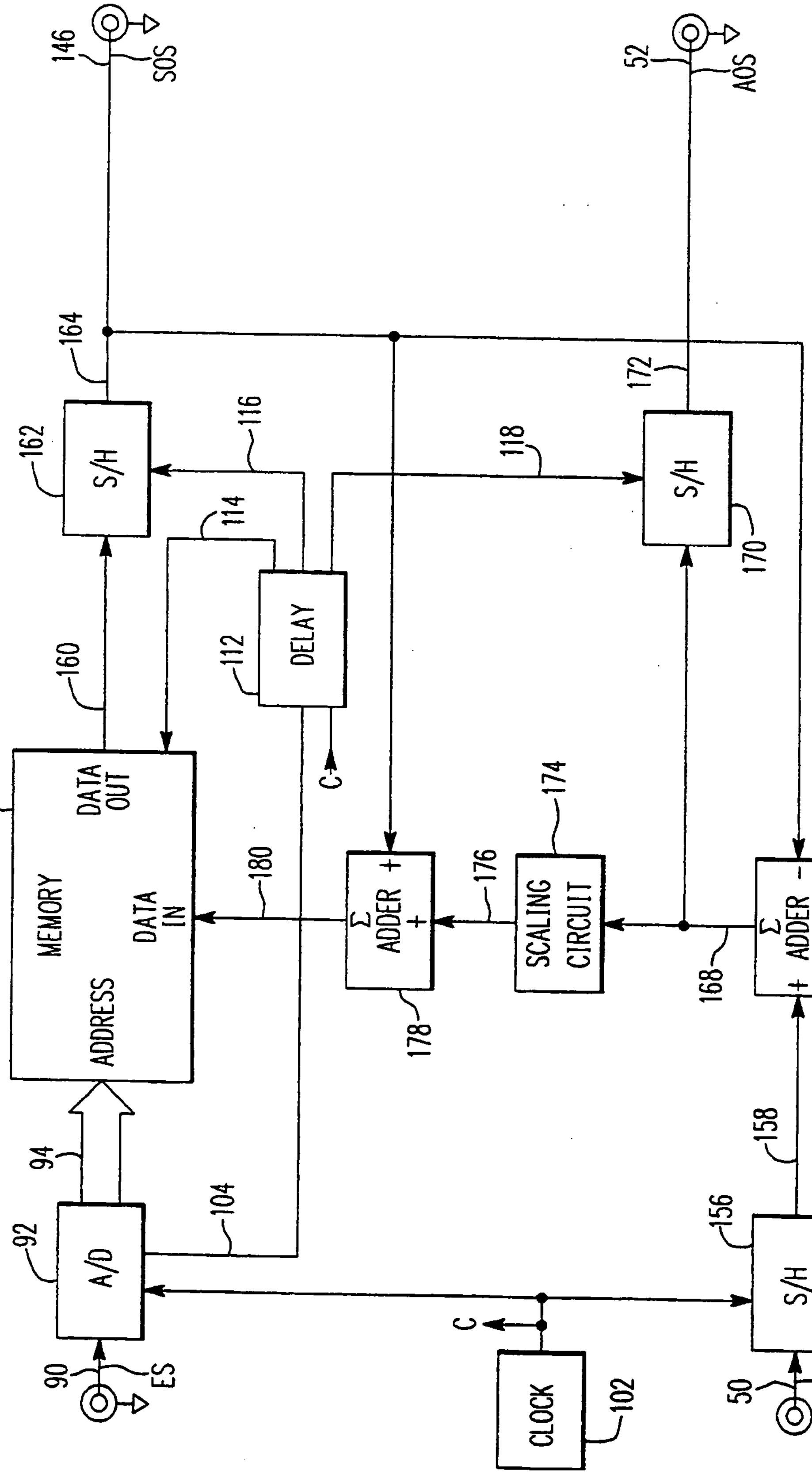
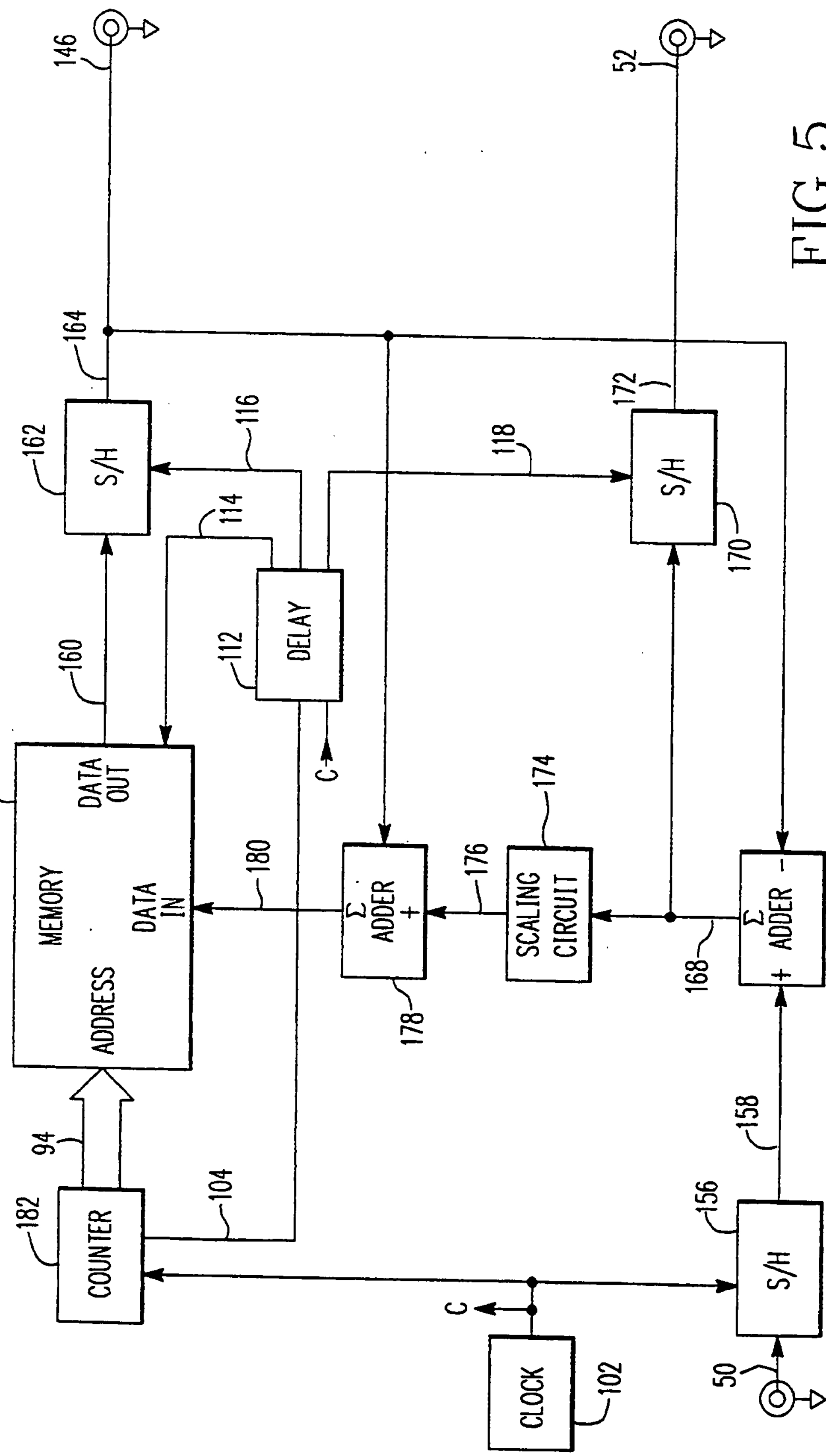

146
SOS
52
AOS
164
172
162
S/H
116
118
S/H
170
114
112
DELAY
160
154
MEMORY
DATA OUT
DATA IN
ADDRESS
C
180
Σ ADDER + +
178
176
SCALING CIRCUIT
174
168
Σ ADDER + -
166
94
104
92
A/D
90
ES
C
CLOCK
102
156
S/H
158
50
SOI+I

FIG. 4



146
52
164
162
S/H
116
114
118
172
S/H
170
DELAY
112
160
154
MEMORY
ADDRESS
DATA IN
DATA OUT
C
174
180
Σ ADDER +
176
SCALING CIRCUIT
Σ ADDER + −
168
166
178
94
182
COUNTER
104
156
S/H
158
C
CLOCK
102
50

FIG. 5

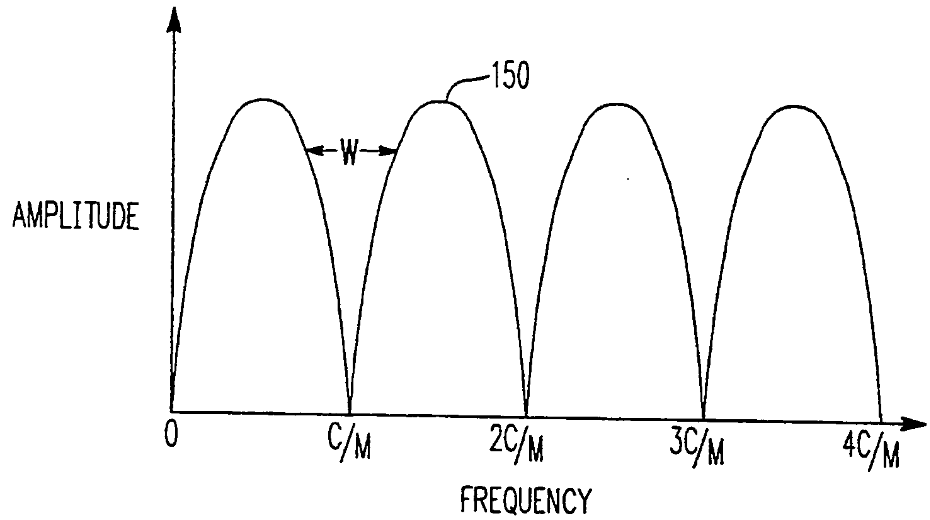
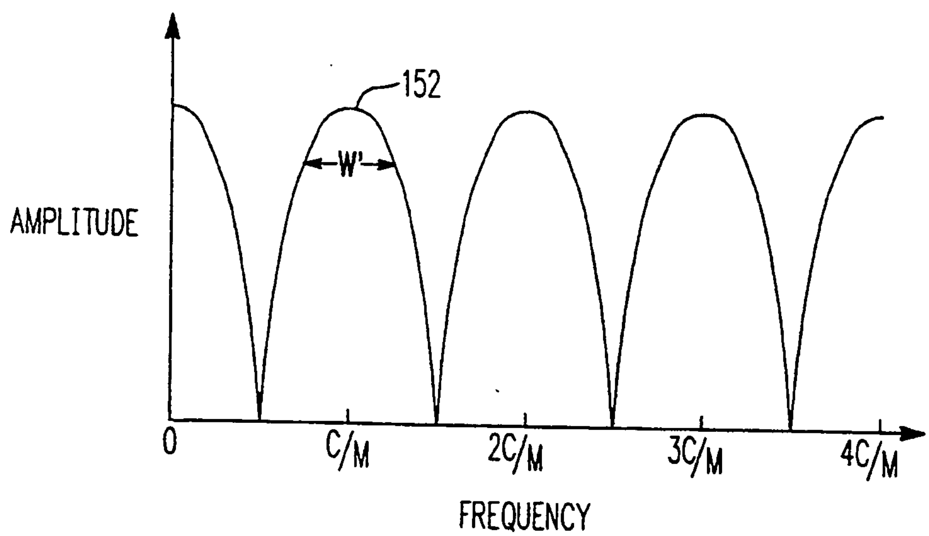

150
W
AMPLITUDE
0
C/M
2C/M
3C/M
4C/M
FREQUENCY

FIG. 6


152
W'
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0
C/M
2C/M
3C/M
4C/M
FREQUENCY

FIG. 7

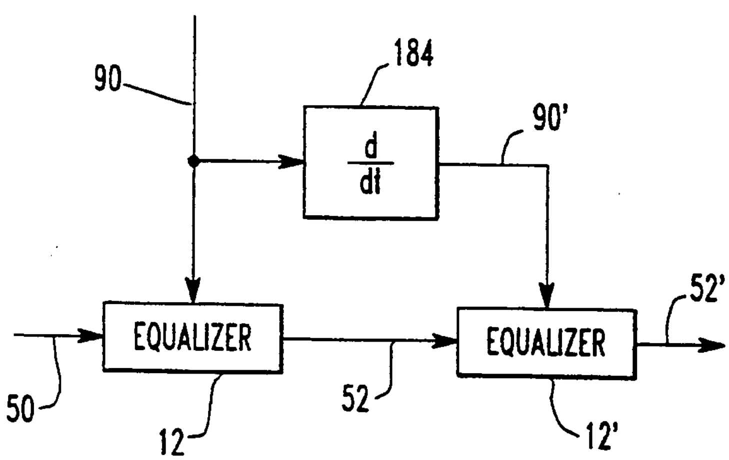

FIG. 8

METHOD AND CIRCUIT FOR PROCESSING AND FILTERING SIGNALS

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation-in-part of allowed application Ser. No. 07/806,058, filed Dec. 11, 1991, and entitled "Method And Circuit For Processing And Filtering Signals" now U.S. Pat. No. 6,263,191.

BACKGROUND OF THE INVENTION

This invention relates to methods and circuits for processing and filtering signals. Such methods and circuits can be particularly adapted to reduce amplitude variations in angle modulated radio frequency signals, or to provide comb notch filtering that removes interference of a repetitive nature.

Multipath phenomena results from multiple paths taken by a transmitted radio frequency signal before the signal reaches a receiver. Transmission of the signal along these paths results in constructive and destructive interference which causes amplitude variations that are a function of the signal's instantaneous frequency. These variations in amplitude complicate subsequent signal processing. For example, in the reception of radio frequency signals, a situation is frequently encountered in which a weak signal of interest (SOI) is subject to interference by a strong interfering signal having a frequency band which encompasses that of the SOI. The interfering signal may be, for example, a jamming signal or a commercial radio or television signal. If the interfering signal is an angle modulated signal, variations in amplitude whether caused by multipath phenomena or otherwise, can further mask the signal of interest, making detection of the signal of interest more difficult.

Interference of a repetitive nature can also cause harmonic interference, in which case it is desirable to remove the harmonic components of a signal. A comb notch filter may be used for such purposes.

The present invention seeks to provide a method and circuit for processing radio frequency signals to filter the signals or to remove the effects of amplitude variations wherein the amplitude variations are correlated with the instantaneous frequency of the signal.

SUMMARY OF THE INVENTION

A circuit for processing electrical signals constructed in accordance with this invention includes: a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal; means for selecting one of the first data signals in response to a second input signal; means for combining the selected one of the first data signals with a second data signal representative of a subsequent instantaneous amplitude of the first input signal, to produce a difference signal; means for producing a first output signal in response to the difference signal; and means for combining the difference signal and the selected one of the first data signals to produce a modified data signal and for replacing the selected first data signal with the modified data signal in the memory.

This invention further encompasses the use of two of the above circuits connected in series, or cascade, wherein the second input signal of one of the circuits is

a first, second or higher order derivative of the second input signal of the other one of the circuits.

The above circuit can serve as an equalizer circuit for removing, or compensating for, the effects of amplitude variations in a radio frequency signal, constructed in accordance with this invention which comprises: a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal, wherein the amplitude variations are correlated with the instantaneous frequency of the signal; a first analog to digital converter for producing an address signal for selecting one of the first data signals in response to a first input signal, the first input signal being correlated with the interfering signal; a first adder for combining the selected one of the first data signals with a second data signal representative of a subsequent instantaneous amplitude of the composite signal, to produce a difference signal; and a second adder for combining the difference signal and the selected one of the first data signals to produce a modified data signal and for replacing the selected one of the first data signals with the modified data signal in the memory. The data signals used in this invention can be either digital signals or sampled analog signals. If digital signals are used, a first digital to analog converter can be used to produce a first analog output signal in response to the difference signal. If sampled analog signals are used, the difference signal can serve as the output signal, or the output signal can be a signal representative of the difference signal.

The invention also includes a method for processing electrical signals comprising the steps of: providing a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal; selecting one of the first data signals in response to a second input signal; combining the selected one of the first data signals with a second data signal representative of a subsequent instantaneous amplitude of the first input signal, to produce a difference signal; and combining the difference signal and the selected one of the first data signals to produce a modified data signal and for replacing the selected one of the first data signals with the modified data signal in the memory. If digital signals are used, a first analog output signal can be produced in response to the difference signal. If sampled analog signals are used, the difference signal can serve as the output signal, or the output signal can be a signal representative of the difference signal.

The invention further encompasses the method for compensating for amplitude variations in an angle modulated radio frequency signal, comprising the steps of: providing a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a composite signal, wherein the composite signal includes a signal of interest and an interfering signal; selecting one of the first data signals in response to a first input signal, the first input signal being correlated with the interfering signal; combining the selected one of the first data signals with a second data signal representative of a subsequent instantaneous amplitude of the composite signal, to produce a difference signal; combining the difference signal and the selected one of the first data signals to produce a modified data signal; and replacing the selected one of the first data signals with the modified data signal in the memory. If digital signals are used, a first analog output signal can be produced in response to the difference

signal. If sampled analog signals are used, the difference signal can serve as the output signal, or the output signal can be a signal representative of the difference signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will become more readily apparent to those skilled in the art through the following description of the preferred embodiment thereof, as illustrated in the drawings, wherein:

FIG. 1 is a block diagram of an interference suppression circuit which includes an equalization circuit constructed in accordance with this invention; and

FIG. 2 is a block diagram of a first embodiment of the equalization circuit of FIG. 1;

FIG. 3 is a block diagram of a first embodiment of a filter circuit constructed in accordance with this invention;

FIG. 4 is a block diagram of a second embodiment of the equalization circuit of FIG. 1;

FIG. 5 is a block diagram of a second embodiment of a filter circuit constructed in accordance with this invention;

FIGS. 6 and 7 are diagrams which illustrate the operation of the filter circuits of FIGS. 3 and 5; and

FIG. 8 is a block diagram of a cascade arrangement of equalizer circuits which may be used in the circuit of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawings, FIG. 1 is a block diagram of an interference suppression circuit 10, having an equalization circuit 12 constructed in accordance with this invention. The circuit of FIG. 1 provides non-cooperative suppression of high-level interference signals to enhance the detection of a co-channel low-level signal of interest (SOI). In this context, non-cooperative suppression refers to suppression of an interfering signal which does not require a reference sample of the interfering signal. The circuit operates on an interference corrupted signal to produce an enhanced version of the desired SOI. The circuit of this invention can be readily retrofitted within the intermediate frequency (IF) stage of existing receiver systems.

A composite signal, including both an angle modulated interfering signal (I) and a signal of interest (SOI) is supplied to the interference suppression circuit 10 by way of input line 14. A signal splitter 16 splits the composite signal and delivers it to a first channel 18 and a second channel 20. An error signal on line 22 is amplified by amplifier 24 and used by a voltage controlled oscillator 26 to produce a reference signal on line 28. The reference signal on line 28 is split by a splitter 30 and sent to first and second in-phase/quadrature splitters 32 and 34, respectively. The in-phase/quadrature splitters produce a first output which is the in-phase component of the reference signal (0 degrees) and a second output which is the quadrature component of the reference signal (90 degrees). A first mixer 36 mixes the composite signal on line 38 with the in-phase component of the reference signal on line 40 to produce a first compound signal on line 42. A filter 44 removes selected components of the first compound signal to produce a first filtered signal on line 46. The filtered signal is delivered via resistor 48 to line 50 where it is combined with a second filtered signal from filter 72 and passed to equalization circuit 12. The equalization circuit produces a modified signal on line 52 which is delivered via resistor 54 to a second mixer 56. The second mixer mixes the modified signal on line 52 with an in-phase component of the reference signal on line 58 to produce a second compound signal on line 60.

A third mixer 62 mixes the composite signal on line 64 with a quadrature component of the reference signal on line 66 to produce a third compound signal on line 68. The error signal on line 22 is the difference in voltage of the first and third compound signals as produced at the output of summation point 70. A second filter 72, which is matched to filter 44, removes selected components of the third compound signal and produces the second filtered signal on line 74. The second filtered signal is combined with the first filtered signal and delivered to the equalization circuit 12 via resistor 76 and line 50. A fourth mixer 78 receives the modified signal on line 52, via resistor 80 and mixes the modified signal with a quadrature component of the reference signal on line 82 to produce a fourth compound signal on line 84. The second and fourth compound signals are combined by combiner 86 to produce an output signal on line 88. The spectral power density of the signal of interest in the output signal is greater than the spectral power density of the interfering signal in the output signal. Therefore the signal of interest in the output signal can be easily captured by well known signal capture circuits. The amplified error signal on line 90 is correlated with the interfering signal portion of the first and second filtered signals. This correlated signal is used to select addresses in a memory of the equalizer as is discussed below. The error signal that drives the VCO is proportional to the instantaneous frequency of the VCO and the interfering signal.

The circuit of FIG. 1 is particularly directed to those instances where the angle modulated interfering signal (I) has a constant envelope with a bandwidth encompassing that of the signal of interest (SOI). The interfering signal may have an inherent amplitude variation which is dependent upon the amount of angle modulation, and will have additional amplitude variation due to multipath phenomena. This amplitude modulation is relatively well defined. The circuit of FIG. 1 is provided as an example of the type of circuit which can benefit from the addition of the equalization circuit of this invention. A detailed description of the operation of the circuit of FIG. 1 is not required in order to practice the present invention, since the invention can be applied to a wide variety of circuits in which an angle modulated signal is subject to undesired amplitude variations.

FIG. 2 is a block diagram of a first embodiment of an equalization circuit constructed in accordance with this invention, and suitable for use as the equalization circuit in FIG. 1. Circuits constructed in accordance with the equalization circuit of FIG. 2 estimate the amplitude variation signature in the interfering signal and subtract it from the filtered signals to reduce the amount of amplitude variation in the resulting modified filtered signal. The estimation is accomplished by repeatedly sampling the input signal and combining the sampled value with a previously stored value to obtain an updated value which replaces the previously stored value. The updated value is typically closer to the previously stored value than the sampled value. In FIG. 2, a first analog to digital converter 92 receives the error signal (ES) on line 90. The error signal is correlated with an interfering signal wherein the interfering signal is one component of a composite signal on line 50. The composite signal on line 50 also includes a signal of interest.

Analog to digital converter 92 produces a digital output signal, representative of the instantaneous amplitude of the signal on line 90, on data bus 94. The data signal on line 94 is used to select an address in memory 96. As is explained below, memory 96 includes a plurality of addresses for storing first digital data signals which are representative of the previous values of the composite signal.

A second analog to digital converter 98 receives the composite signal, including both the interfering signal (I) and the signal of interest (SOI) on line 50, and produces a digital output signal on line 100 that is representative of the instantaneous value of the composite signal. Clock 102 controls the sequence of operations performed by the circuit of FIG. 2. In response to a predetermined change in polarity of the output pulses of clock 102, analog to digital converters 92 and 98 produce their respective output signals. The analog to digital converters also produce data ready signals on lines 104 and 106. These data ready signals are received by AND gate 108 and used to produce a voltage pulse on line 110. The voltage pulse on line 110 passes to delay circuit 112, which may be a shift register. Delay circuit 112 then produces output pulses on lines 114, 116 and 118. The first data signal is selected by the address identified by the signal on bus 94, and read out onto bus 120. Alternatively, selection of the first data signal may be done utilizing a software loop. The selected signal is then frozen by latch 122, which is controlled by a pulse on line 116. The frozen signal on bus 124 is delivered to adder 126 where it is subtracted from the signal on bus 100 to produce a digital difference signal on bus 128. Latch 130 freezes the digital difference signal on bus 132 in response to a voltage pulse on line 118. A first digital to analog converter 134 converts the digital signal on bus 132 to an analog output signal (AOS) on line 52. When this circuit is used in the circuit of FIG. 1, the output signal from digital to analog converter 134 is the modified filtered signal.

Scaling circuit 136 divides the digital difference signal on bus 128 by a preselected number to produce an incremental adjustment signal on bus 138. The incremental adjustment signal on bus 138 is then added to the first digital data signal on bus 124 to adder 140 to obtain a modified digital data signal on bus 142. A pulse on line 114 enables memory 96 to replace the selected first digital data signal previously read from the memory with the digital data signal on bus 142 at the address identified by the signal on bus 94. A second digital to analog converter 144 converts the first digital signal on bus 124 into a second output signal (SOS) on line 146. The second output signal (which is not used by the circuit of FIG. 1) is representative of the interfering signal component of the composite signal.

The circuit of FIG. 2 uses a successive estimation technique to update the data in the memory so that the stored data approaches an accurate representation of the amplitude modulation of the interfering signal. The amount by which the values of the stored data are adjusted (attack rate) is controlled by changing the value of the divisor in scaling circuit 136. The input signal on line 50 is a composite signal which includes a signal of interest and an undesired interfering signal, wherein the signal of interest can be considered to be a deviation from the average of the composite signal. The input signal on line 90 is a signal which is correlated with the interfering signal. The output signal on line 52 is an uncorrelated amplitude modulated signal which is representative of the signal of interest. The output signal on line 146 is a correlated amplitude modulated signal representative of the interfering signal.

FIG. 3 is a block diagram of a comb notch filter which uses the circuit of this invention. This circuit is similar to the circuit of FIG. 2 except that the analog to digital converter 92 in FIG. 2 has been replaced by a counter 148. The signal to be filtered is applied to input line 50. Clock 102 controls the sampling rate of analog to digital converter 98 and also increments the counter to provide an address location on bus 94.

FIG. 4 is a block diagram of a second embodiment of an equalization circuit constructed in accordance with this invention, and suitable for use as the equalization circuit in FIG. 1. As is the case for circuits constructed in accordance with the equalization circuit of FIG. 2, the circuit of FIG. 4 estimates the amplitude variation signature in the interfering signal and subtracts it from the filtered signals to reduce the amount of amplitude variation in the resulting modified filtered signal. The estimation is accomplished by repeatedly sampling the input signal and combining the sampled value with a previously stored value to obtain an updated value which replaces the previously stored value. The updated value is typically closer to the previously stored value than the sampled value. In FIG. 4, an analog to digital converter 92 receives the error signal (ES) on line 90. The error signal is correlated with an interfering signal wherein the interfering signal is one component of a composite signal on line 50. The composite signal on line 50 also includes a signal of interest. Analog to digital converter 92 produces a digital output signal, representative of the instantaneous amplitude of the signal on line 90, on data bus 94. The signal on bus 94 is used to select an address in memory 154. Memory 154 is an analog memory, which may include, for example, a charge coupled device array or a switched capacitor array. Memory 154 includes a plurality of addresses for storing first data signals which are representative of the previous sampled values of the composite signal.

A first sample and hold circuit 156 receives the composite signal, including both the interfering signal (I) and the signal of interest (SOI), on line 50, and produces a sampled analog output signal on line 158 that is representative of the instantaneous value of the composite signal. Clock 102 controls the sequence of operations performed by the circuit of FIG. 4. In response to a predetermined change in polarity of the output pulses of clock 102, analog to digital converter 92 and sample and hold circuit 156 produce their respective output signals. The analog to digital converter 92 also produces a data ready signals on line 104. This data ready signal passes to delay circuit 112. Delay circuit 112 then produces output pulses on lines 114, 116 and 118. The first data signal is selected by the address identified by the signal on bus 94, and read out onto line 160. The selected signal is then frozen by sample and hold circuit 162, which is controlled by a pulse on line 116. The frozen signal on line 164 is delivered to analog adder 166 where it is subtracted from the signal on line 158 to produce a difference signal on line 168. Sample and hold circuit 170 freezes the difference signal on line 172 in response to a voltage pulse on line 118. The frozen difference signal serves as the analog output signal (AOS) on line 52. When this circuit is used in the circuit of FIG. 1, the output signal is the modified filtered signal.

Scaling circuit 174 attenuates the difference signal on line 168 by a preselected amount to produce an incre-

mental adjustment signal on line **176**. The incremental adjustment signal on line **176** is then added to the first data signal on line **164** by adder **178** to obtain a modified data signal on line **180**. A pulse on line **114** enables memory **154** to replace the selected first data signal previously read from the memory with the data signal on line **180** at the address identified by the signal on bus **94**. The data signal on line **164** serves as a second output signal (SOS) on line **146**. The second output signal (which is not used by the circuit of FIG. **1**) is representative of the interfering signal component of the composite signal.

The circuit of FIG. **4** uses a successive estimation technique to update the data in the memory so that the stored data approaches an accurate representation of the amplitude modulation of the interfering signal. The amount by which the values of the stored data are adjusted (attack rate) is controlled by changing the amount of attenuation provided by scaling circuit **174**. The input signal on line **50** is a composite signal which includes a signal of interest and an undesired interfering signal, wherein the signal of interest can be considered to be a deviation from the average of the composite signal. The input signal on line **90** is a signal which is correlated with the interfering signal. The output signal on line **52** is an uncorrelated amplitude modulated signal which is representative of the signal of interest. The output signal on line **146** is a correlated signal representative of the amplitude modulation of the interfering signal.

It should be apparent that the various embodiments of this invention can enhance the interception of low-level signals of interest in the presence of strong interference by reducing the interference due to amplitude variations in the interfering signal which tend to mask the signal of interest. The invention is also useful in circuits used to suppress co-site/co-channel interference in tactical and strategic communications systems.

The distorted version of interfering signal Y, present on line **50** or bus **100**, can be represented as a polynomial of the form:

$$Y = \sum_{n=0}^{\infty} C_n X^n$$

where X is the interfering signal or value on line **90** or bus **94**. The circuits of this invention learn the coefficients C_n of the terms of the polynomial and subtract those terms from the composite signal, within the limits of the digital quantization. This is accomplished by using a memory having individual bins for each level of the interfering signal, thereby permitting each level to be handled separately.

FIG. **5** is a block diagram of an analog comb notch filter which uses the circuit of this invention. This circuit is similar to the circuit of FIG. **4** except that the analog to digital converter **92** in FIG. **4** has been replaced by a counter **182**. The signal to be filtered is applied to input line **50**. Clock **102** controls the sampling rate of the sample and hold circuit **156** and also increments the counter to provide an address location on bus **94**. The circuits of FIGS. **3** and **5** each produce an output on line **52** which is an uncorrelated notched output and is illustrated in FIG. **6**, wherein C is the clock frequency and M is the maximum address on the data bus **94**. The amplitude in FIG. **6** is the ratio of the amplitudes of the signals on line **52** and **50** as a function of frequency. The width of the notch W is directly proportional to the C/M ratio and inversely proportional to the sealing factor in block **136**. The output on line **146** is a correlated bandpass output and is illustrated in FIG. **7**, wherein C is the clock frequency and M is the maximum address on the data bus **94**. The amplitude in FIG. **7** is the ratio of the amplitudes of the signals on lines **146** and **50**. The width of the passband W' is directly proportional to the C/M ratio and inversely proportional to the sealing factor in block **136**.

FIG. **8** is a block diagram of a cascade connection of equalizers which may be used in the circuit of FIG. **1**. In this Figure, equalizer **12'** is identical to equalizer **12**, except that the error signal on line **90'** which is delivered to equalizer **12'** is the first derivative with respect to time of the error signal on line **90**. This derivative is produced by a differentiation circuit as illustrated by block **184**. Although the first derivative is used in this example, it should be understood that higher order derivatives may also be used. The circuit of FIG. **8** may be inserted into the circuit of FIG. **1**, with the output **52'** of equalizer **12'** being connected to the junction point between resistors **54** and **80**. By using a second, series connected equalizer having a derivative of the error signal as an input, improved performance can be achieved. As the rate of change of frequency of the interfering signal increases, some of the signal components relating to amplitude envelope variations become more significant. Since the correlation of the error signal with the instantaneous frequency of the interfering signal becomes less accurate as the multipath delay increases, the use of an error signal which is related to the derivative of the instantaneous frequency can provide improved performance. The derivative of the error signal may be taken with respect to time or another parameter, such as frequency.

Although the invention has been described in terms of its preferred embodiments, it will be apparent to those skilled in the art that various changes may be made without departing from the scope of the invention. It is therefore intended that the appended claims cover such changes.

I claim:

1. A circuit for processing electrical signals comprising:

a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal;

means for selecting one of said first data signals in response to a second input signal;

means for combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said first input signal, to produce a difference signal;

means for producing a first output signal in response to said difference signal; and

means for combining said difference signal and the selected one of the first data signals to produce a modified data signal and for replacing the selected one of the first data signals with said modified data signal in said memory.

2. A circuit for processing electrical signals according to claim **1**, wherein:

the first input signal includes a signal of interest and an interfering signal; and

said interfering signal being correlated with said second input signal.

3. A circuit for processing electrical signals according to claim 1, further comprising:

means for producing a second output signal in response to the selected one of said first data signals.

4. A circuit for processing electrical signals according to claim 1, wherein said means for combining said difference signal and the selected one of said first data signals to produce a modified data signal and for replacing the selected one of said first data signals with said modified data signal in said memory, comprises:

a scaling circuit for attenuating said difference signal by a preselected amount to produce a correction signal; and

an adder adding said correction signal to the selected first data signal to produce said modified data signal.

5. A circuit for processing electrical signals according to claim 1, wherein said means for selecting one of said first data signals in response to a second input signal comprises:

a counter for producing said second input signal in response to a clock signal.

6. A method for processing electrical signals comprising the steps of:

providing a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal;

selecting one of said first data signals in response to a second input signal;

combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said first input signal, to produce a difference signal;

producing a first output signal in response to said difference signal; and

combining said difference signal and the selected one of said first data signals to produce a modified data signal and replacing the selected one of said first data signals with said modified data signal in said memory.

7. A method for processing electrical signals according to claim 6, wherein:

the first input signal includes a signal of interest and an interfering signal; and

said interfering signal is correlated with said second input signal.

8. A method for processing electrical signals according to claim 6, further comprising the step of:

producing a second output signal in response to the selected one of said first data signals.

9. A method for processing electrical signals according to claim 6, wherein said step of combining said difference signal and the selected one of said first data signals to produce a modified data signal and for replacing the selected one of said first data signals with said modified data signal in said memory, comprises the steps of:

attenuating said difference signal by a preselected amount to produce a correction signal; and

adding said correction signal to the selected one of said first data signals to produce said modified data signal.

10. A circuit for compensating for amplitude variation in an angle modulated composite signal comprising:

a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of the composite signal, wherein the composite signal includes a signal of interest and an interfering signal;

means for selecting one of said first data signals in response to a second input signal, said interfering signal being correlated with said second input signal;

means for combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said composite signal, to produce a difference signal;

means for producing a first analog output signal in response to said difference signal; and

means for combining said difference signal and the selected one of said first data signals to produce a modified data signal and for replacing the selected one of said first data signals with said modified data signal in said memory.

11. A circuit for compensating for amplitude variation in an angle modulated composite signal according to claim 10, further comprising:

means for producing a second output signal in response to the selected one of said data signals.

12. A circuit for compensating for amplitude variation in an angle modulated composite signal according to claim 10, wherein said means for combining said difference signal and the selected one of said first data signals to produce a modified data signal and for replacing the selected one of said first data signals with said modified data signal in said memory, comprises:

a scaling circuit for attenuating said difference signal by a preselected amount to produce a correction signal; and

an adder adding said correction signal to the selected one of said first data signals to produce said modified data signal.

13. A circuit for compensating for amplitude variation in an angle modulated composite signal comprising:

a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of the composite signal, wherein the composite signal includes a signal of interest and an interfering signal;

a first analog to digital converter producing an address signal for selecting one of said first data signals in response to a second input signal, said second input signal being correlated with said interfering signal;

a first adder for combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said composite signal, to produce a difference signal;

means for producing a first analog output signal in response to said difference signal; and

a second adder for combining said difference signal and the selected one of said first data signals to produce a modified data signal and for replacing the selected one of said first data signals with said modified data signal in said memory.

14. A circuit for compensating for amplitude variation in an angle modulated composite signal according to claim 13, further comprising:

means for producing a second output signal in response to the selected one of said data signals.

15. A method for compensating for amplitude variation in an angle modulated composite signal, said method comprising the steps of:

providing a memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of the composite signal, wherein the composite signal includes a signal of interest and an interfering signal;

selecting one of said first data signals in response to a second input signal, said second input signal being correlated with said interfering signal;

combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said composite signal, to produce a difference signal;

producing a first analog output signal in response to said difference signal;

combining said difference signal and the selected one of said first data signals to produce a modified data signal; and

replacing the selected one of said first data signals with said modified data signal in said memory.

16. A method for compensating for amplitude variation in an angle modulated composite signal according to claim 15, further comprising the step of:

producing a second output signal in response to the selected one of said data signals.

17. A method for compensating for amplitude variation in an angle modulated composite signal according to claim 15, wherein said step of combining said difference signal and the selected one of said first data signals to produce a modified data signal, comprises the steps of:

attenuating said difference signal by a preselected amount to produce a correction signal; and

adding said correction signal to the selected one of said first data signals to produce said modified data signal.

18. A circuit for processing electrical signals comprising:

a first equalizer including a first memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal; means for selecting one of said first data signals in response to a second input signal; means for combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said first input signal, to produce a first difference signal; means for producing a first output signal in response to said first difference signal; and means for combining said first difference signal and the selected one of the first data signals to produce a first modified data signal and for replacing the selected one of the first data signals with said first modified data signal in said first memory;

a second equalizer including a second memory having a plurality of addresses for storing a plurality of third data signals, each representative of an instantaneous amplitude of said first output signal; means for selecting one of said third data signals in response to a third input signal; means for combining the selected one of said third data signals with a fourth data signal representative of an additional instantaneous amplitude of said first output signal, to produce a second difference signal; means for producing a second output signal in response to said second difference signal; and means for combining said second difference signal and the selected one of the third data signals to produce a second modified data signal and for replacing the selected one of the third data signals with said second modified data signal in said second memory.

19. A circuit for processing electrical signals according to claim 18, wherein said third input signal is representative of a derivative of said second input signal.

20. A circuit for processing electrical signals according to claim 19, wherein said derivative is taken with respect to either time or frequency.

21. A method for processing electrical signals comprising the steps of:

providing a first memory having a plurality of addresses for storing a plurality of first data signals, each representative of an instantaneous amplitude of a first input signal;

selecting one of said first data signals in response to a second input signal;

combining the selected one of said first data signals with a second data signal representative of an additional instantaneous amplitude of said first input signal, to produce a first difference signal;

producing a first output signal in response to said first difference signal;

combining said first difference signal and the selected one of said first data signals to produce a first modified data signal and replacing the selected one of said first data signals with said first modified data signal in said first memory;

providing a second memory having a plurality of addresses for storing a plurality of third data signals, each representative of an instantaneous amplitude of said first output signal;

selecting one of said third data signals in response to a third input signal;

combining the selected one of said third data signals with a fourth data signal representative of an additional instantaneous amplitude of said first output signal, to produce a second difference signal;

producing a second output signal in response to said second difference signal;

combining said second difference signal and the selected one of said third data signals to produce a second modified data signal and replacing the selected one of said third data signals with said second modified data signal in said second memory.

22. A method for processing electrical signals according to claim 21, wherein said third input signal is representative of a derivative of said second input signal.

23. A circuit for processing electrical signals according to claim 22, wherein said derivative is taken with respect to either time or frequency.

* * * * *

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United States Patent [19]

Vagher

[11] **Patent Number: 5,507,036**

[45] **Date of Patent: Apr. 9, 1996**

[54] **APPARATUS WITH DISTORTION CANCELLING FEED FORWARD SIGNAL**

[75] Inventor: **Michael R. Vagher**, Cedar Rapids, Iowa

[73] Assignee: **Rockwell International**, Seal Beach, Calif.

[21] Appl. No.: **316,285**

[22] Filed: **Sep. 30, 1994**

[51] **Int. Cl.**[6] **H04B 1/10**

[52] **U.S. Cl.** **455/295**; 455/304; 455/312; 455/324; 455/326

[58] **Field of Search** 455/295, 296, 455/302, 303, 304, 306, 307, 310, 313, 317, 323, 324, 326, 333, 312; 381/13; 332/145; 333/177; 375/99

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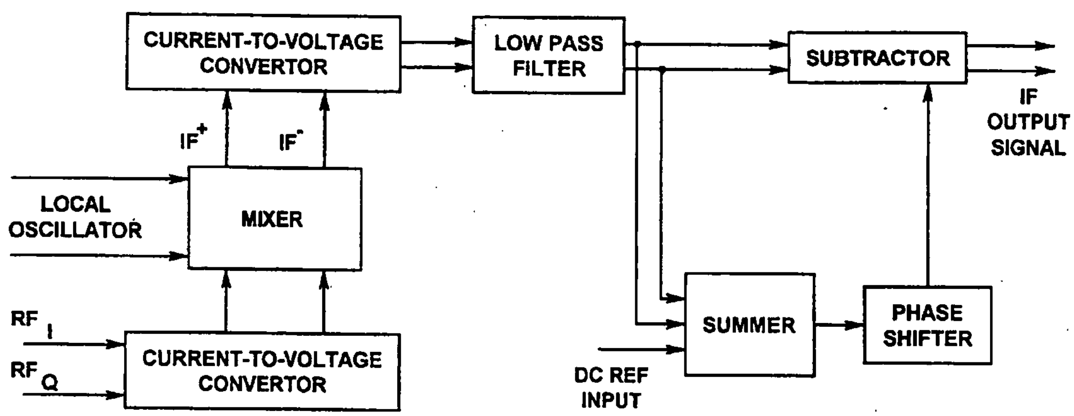
Primary Examiner—Andrew I. Faile

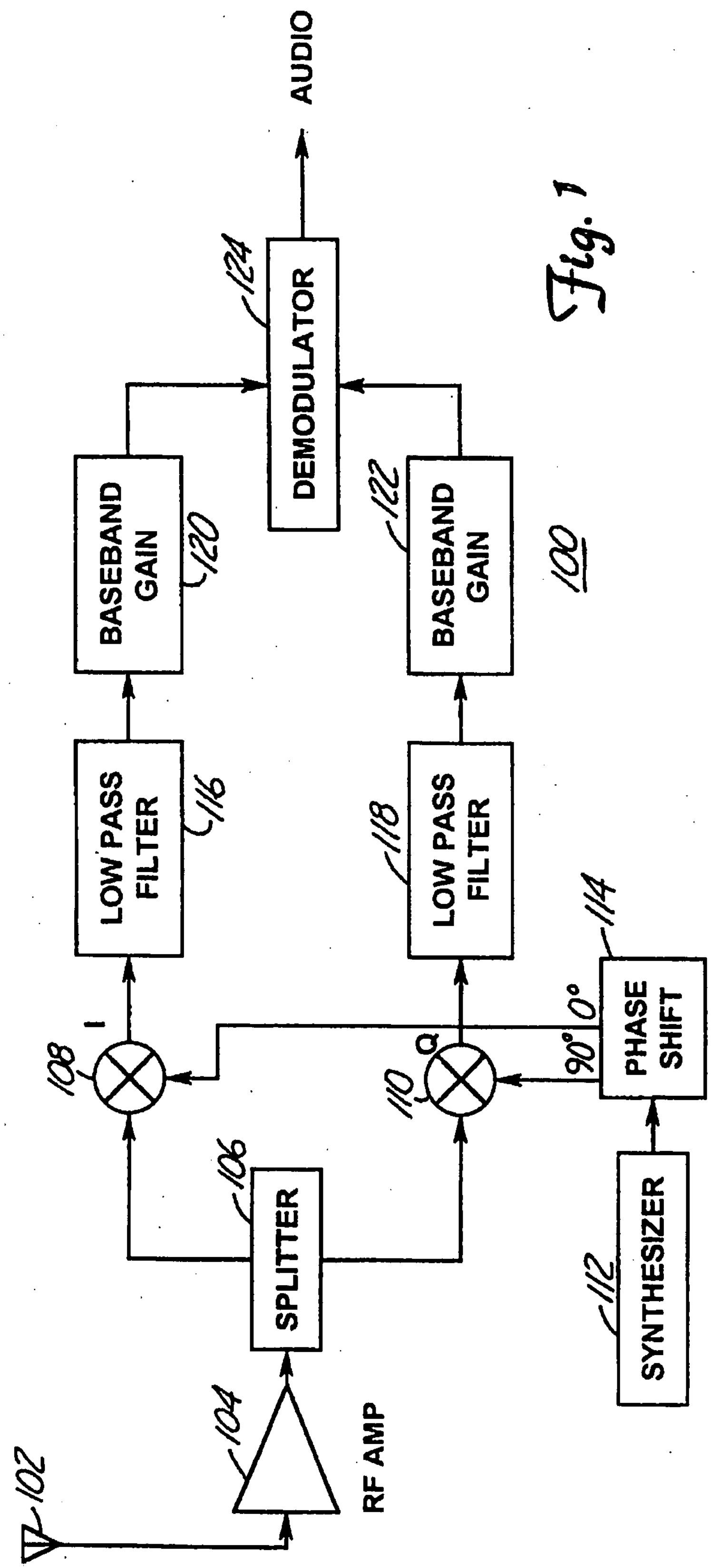
Attorney, Agent, or Firm—Kyle Eppele; M. Lee Murrah; G. A. Montanye

[57] **ABSTRACT**

An apparatus and a method for cancelling distortion in a direct conversion receiver, such distortion created by the mixing of the desired signal with the output signal of an local oscillator. Subsequent to filtering the mixer output signal, the even mode distortion component is extracted, phase shifted, amplified and recombined with the mixed signal in such manner as to suppress even order distortion.

7 Claims, 4 Drawing Sheets




AUDIO
124
DEMODULATOR
BASEBAND GAIN
120
BASEBAND GAIN
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100
LOW PASS FILTER
116
LOW PASS FILTER
118
114
PHASE SHIFT
0°
90°
I
Q
108
110
106
SPLITTER
112
SYNTHESIZER
104
RF AMP
102

Fig. 1

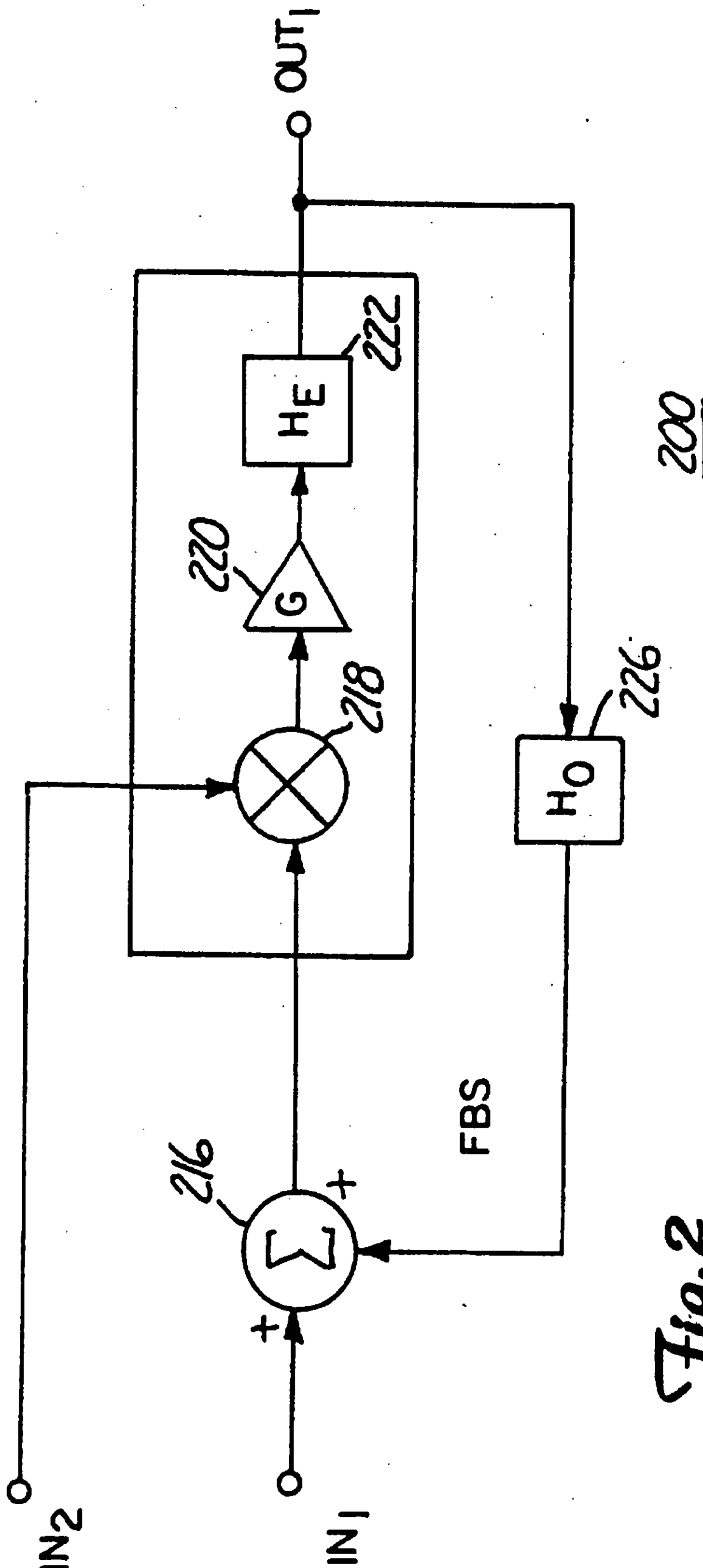

Fig. 2
PRIOR ART

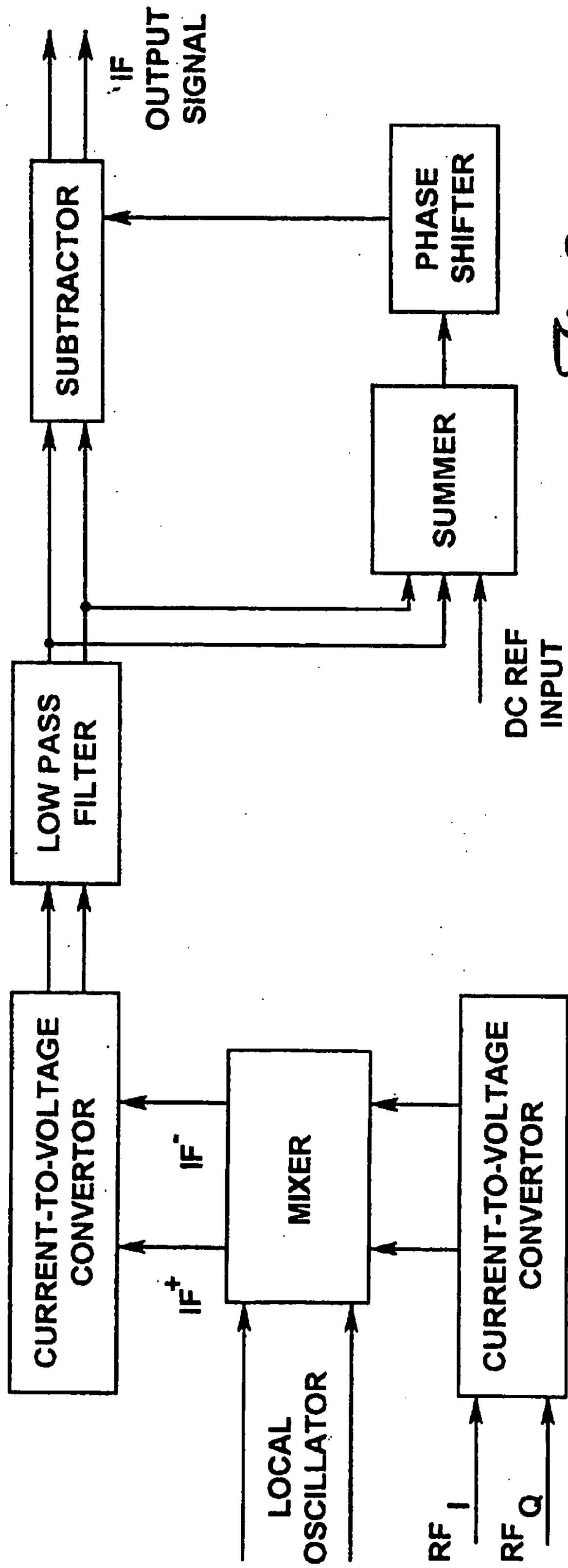
IF OUTPUT SIGNAL
SUBTRACTOR
PHASE SHIFTER
SUMMER
DC REF INPUT
LOW PASS FILTER
CURRENT-TO-VOLTAGE CONVERTOR
IF⁻
IF⁺
MIXER
CURRENT-TO-VOLTAGE CONVERTOR
LOCAL OSCILLATOR
RF I
RF Q

Fig.3

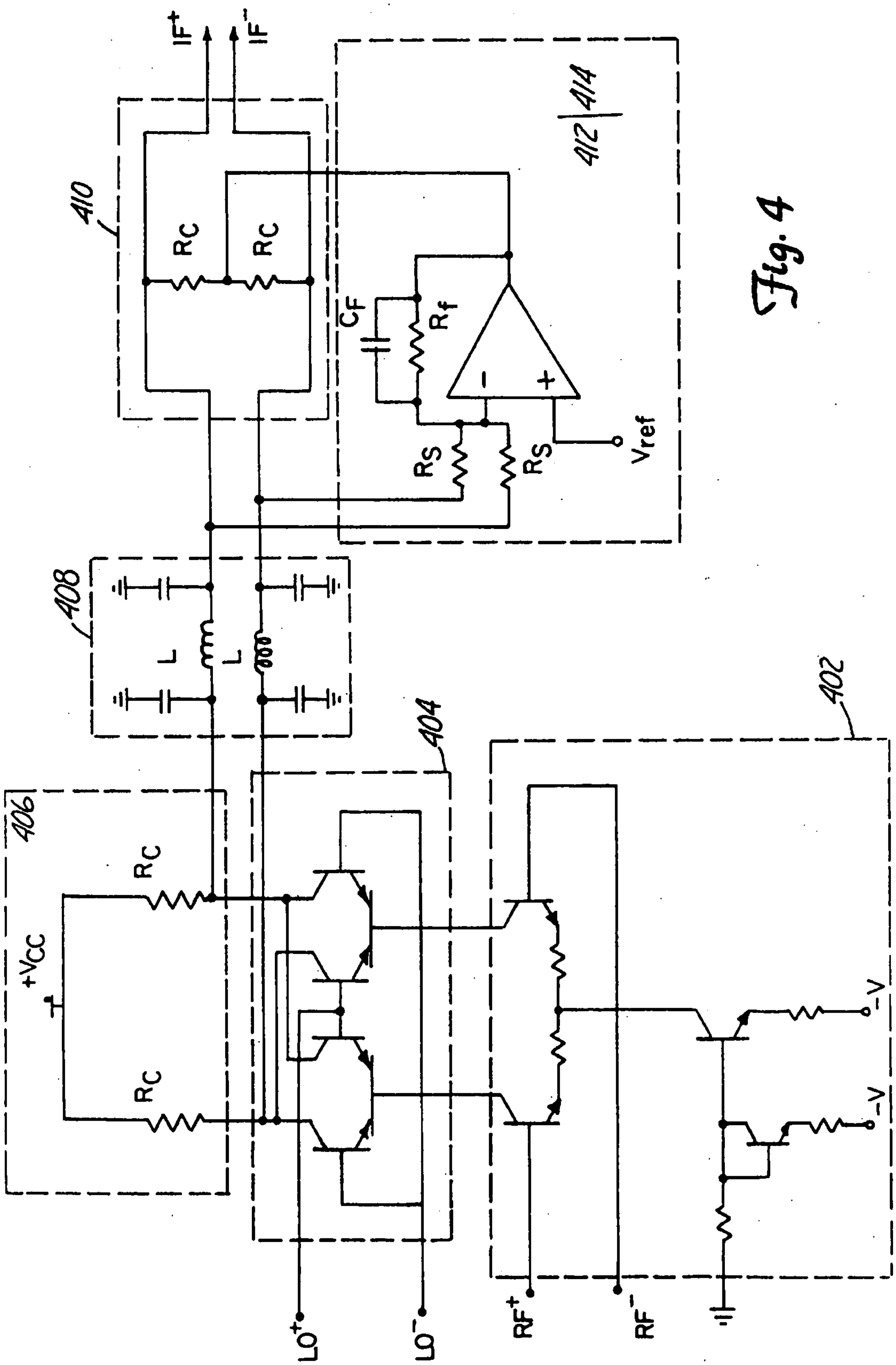
IF+
IF−
410
412|414
RC
RC
CF
Rf
RS
RS
Vref
408
L
L
406
RC
+VCC
RC
404
402
−V
−V
LO+
LO−
RF+
RF−

Fig. 4

APPARATUS WITH DISTORTION CANCELLING FEED FORWARD SIGNAL

BACKGROUND OF THE INVENTION

The present invention relates to electronic circuits and more particularly to electronic circuits using open loop control signals to minimize distortion.

Conventional mixers are widely used in a variety of electronic circuitry such as radios, cellular telephones or other devices, requiring the product of two waveform signals. Such mixers typically produce an output signal at a frequency that is the sum, or difference, of the two incoming signal frequencies. This output signal or "mixed" signal undergoes further processing to demodulate the desired data that is typically modulated on one of the signals. Prior art mixers can produce output signals having undesired components including direct current ("DC") caused by a non-linear response of the mixer. An ideal mixer would form the product of two signals and not have these secondary non-linear responses. Some applications are less tolerant of accommodating such undesired signal components.

A direct conversion receiver ("DCR") is one such application where undesired signals from the mixer can render the receiver non-functioning. Typically, a DCR uses a balanced mixer that receives a radio frequency ("RF") signal and a local oscillator signal. The local oscillator and RF signal are at the same frequency and therefore the modulation on the RF signal is converted directly to baseband. In the presence of a strong applied RF signal which is off-channel or an undesired interfering signal, the second order distortion component in the non-linear device which comprises the mixer causes a second harmonic and also creates a DC with an unmodulated RF signal, or a conversion of the modulated signal to baseband with a carrier signal that is amplitude modulated. Since the desired RF signal is also converted to zero IF and the modulation to baseband, this can interfere with the desired signal. This problem is often referred to as a spurious demodulation phenomena or direct detection. The undesired RF signal is directly detected or demodulated through second order distortion, not through mixing action, and thus is demodulated (if signal is strong) regardless of signal frequency.

SUMMARY OF THE INVENTION

The present invention comprises an apparatus and method that minimizes signal distortion in a processed modulated radio signal by use of a feed forward correction signal generated and determined beyond the mixer stage of the receiver. In one embodiment of the present invention an RF input signal is mixed with the output of a local oscillator and subsequently converted to a voltage equivalent, the signal may then be passed through a low pass filter. An even mode distortion extractor is coupled to the output of the low pass filter. The extractor also receives a reference input signal and generates as its output, a signal that contains even order distortion. This output signal is then phase shifted and coupled to a summer which combines the correction signal to the signal that is generated by the low pass filter. It is worth noting, that unlike numerous prior art solutions the present invention generates a correction signal and implements the same signal at a point in the processing stage beyond the mixer.

It is an object of the present invention to provide a radio receiver having improved reception qualities due to increased distortion suppression.

It is a feature of the present invention to utilize a feed forward correction signal based upon an even mode distortion extraction technique.

It is an advantage of the present invention that a desired component of a process signal can be effectively separated from an undesired component thereby yielding a superior output value.

These and other objects, features and advantages are disclosed and claimed in the specification, figures and claims of the present application.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a direct conversion receiver capable of incorporating the teachings of the present invention;

FIG. 2 is a block diagram of a prior art feed back mixer;

FIG. 3 is a block diagram of the teachings of the present invention; and

FIG. 4 is a schematic diagram of a mixer utilizing the teachings of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the Figures, wherein like numbers are referenced as such throughout, FIG. 1 illustrates a direct conversion receiver **100** capable of benefiting from the teachings of the present invention. The receiver **100** would typically include an RF amplifier **104** and a splitter **106** for dividing an incoming RF communication signal into a pair of equal and inphase components. The RF signal components are combined at the mixers **108**, **110** with separate injection signals on frequency with the communications signal but separated by a phase difference of 90°. Inphase and quadrature baseband signal components are formed which are independently filtered and amplified at audio frequencies on separate signal channels by separate filters **116**, **118** and amplifiers **120**, **122**. The inphase and quadrature components formed as a result of the mixing process allow the signal to be conveniently and accurately demodulated upon being supplied to a suitable signal processing unit **124** such as a demodulator.

FIG. 2 shows an active filtering mixer **200** as known in the prior art. A first input signal IN_1 is coupled to a summer **216**, the output signal of the summer **216** is coupled to a multiplier **218**, the multiplier **218** also receives a second input signal IN_2 thereby performing the mixing of the signals IN_1 and IN_2. The output signal of the multiplier **218** is coupled through an amplifier **220** whose output signal is in turn coupled through a high pass filter **222** thereby yielding an output signal OUT_1. The output signal is also coupled in feedback fashion to the summer unit **216** via feedback selection means **226**. The feedback selection means **226** filters or amplifies dependent upon the specified application to produce a feedback signal FBS which is coupled to summer **216**.

The output of the multiplier **218** can be considered to have a desired component, and superimposed thereon an unwanted component. The feedback signal generated in feedback means **226** is a function of the signal components. Application of the feedback signal FBS to the multiplier **218** causes an unwanted component of its output to be largely suppressed. This result is obtained due to the multiplier **218** generating in its output a cancellation signal that suppresses the unwanted component.

FIG. 3 illustrates a block diagram of a portion of an RF receiver that implements the teachings of the present invention. An RF input signal RF^+, RF^- is shown coupled to a voltage-to-current converter **302**. The output signals of the converter **302** are coupled to a mixer **304** which combines the current RF signal with an input signal from a local oscillator. The mixed signals IF^+ and IF^- are then coupled to a current-to-voltage converter **306**, then in turn coupled to a balanced low pass filter **308**. The output signals of the filter **308** are coupled to a subtractor **310** and an extractor **312**. The extractor also receives a reference input signal from a DC source illustrated as DC_r. The extractor generates a signal that is then coupled through a phase shifter **314** and combined with the output of the filter **308** at the subtractor **310**. The output signals of the subtractor **310** are then coupled to additional processing means not shown.

FIG. 4 illustrates the block diagram of FIG. 3 in schematic format having the blocks superimposed upon the schematic in dashed manner. The Applicant has adhered to conventional electrical symbology for resistors, transistors, capacitors and inductors in presenting the schematic of FIG. 4. The operation of the apparatus of FIGS. 3 and 4 will now be described in detail. The voltage-to-current converter **402**, the mixer **404**, and the current-to-voltage converter **406** may all be implemented in commercially available active mixers manufactured in accordance with well known integrated circuit techniques. The mixer **404** and the low pass filter **408** are in a balanced signal format and must remain so through the rest of the circuit. The filter **408** provides an output signal that contains the desired signal in a DCR application (voice frequency) and may also contain distortion from a strong off-channel undesired signal if present. A critical part of this invention is the use of the difference between the desired signal and distortion. If a strong off-channel or adjacent channel signal is present, the modulation on this signal will be converted to a "baseband" signal through the distortion mechanism of the mixer **404**. The baseband frequency range is usually the same as that of the desired signal. The off-channel signal is not converted to baseband by "mixing" action as is the desired signal. However, it is converted by a "square law" distortion present in the mixer that has behavior much like a diode detector. Therefore, any demodulation of an undesired signal depends not on its frequency but signal strength. Thus an important aspect of this invention is that signal distortion caused by "second order" nonlinearity exists in the mixer **404** in a common-mode form while the desired signal exists in a balanced form.

The distortion and desired signal are not separated in frequency, thus the common-mode, balanced mode difference is the only discriminator easily detected between the two signal components. The conversion from balanced signal to single ended signal will idealy cancel all common-mode signals, thereby rejecting the distortion component of the signal. However, in actuality the rejection is typically on the order of 20 decibels to 30 decibels yielding unacceptable results in DCRs. The distortion component of the output of the balanced low pass filter **408** is best coupled to an extractor **412**, which in actuality is a summer device. This will add the distortion component on each balanced output while cancelling the desired signal component an appreciable amount. The output signal of the extractor **412** is now principally composed of the second order distortion component of the input signal. It is then amplified and phase shifted by 180°. The output signal of the amplifier and phase shifter **414** is then subtracted from the output of filter **408** by device **410**. This is accomplished by applying the output signal of the phase shift device **414** to the midpoint of two resistors of equal value as shown in FIG. 4. By injecting the signal at this point, only the common-mode component of the signal is effected. The Applicant refers to this approach as a feed-forward cancellation because the distortion is cancelled at a point beyond the mixer **404**, where it is generated. It is noted that feed back is used at the actual point of distortion cancellation. The distortion component is amplified by the operational-amplifier shown in FIG. 4 in accordance with the value R_f/R_s. The use of the capacitor C_f provides loop stability. The resultant distortion component signal is then applied to a common-mode subtractor **410**. This then diminishes the distortion that is available to the input of the operational-amplifier. The level of distortion reduction will depend on the value R_f/R_s which can be chosen high enough to reduce the distortion to negligible levels. It is assumed but not shown in the schematics that the IF signal is subsequently converted to a single ended signal.

The above described technique and apparatus will not cancel distortion in a mixer caused by odd-order non-linearities. For this reason the teachings of this application are deemed to be application specific to DCRs where even order distortions (second order being dominant) present a major problem.

Those skilled in the art will readily recognize that various modifications and changes may be made to the present invention without departing from the true spirit and scope thereof, which is set forth in the following claims.

I claim:

1. An apparatus for common-mode extraction of even mode non-linear distortion in a direct conversion receiver, comprising:
   - a mixer that combines an RF input signal with an output signal of a local oscillator;
   - a balanced low-pass filter coupled to an output signal of the mixer;
   - an even mode distortion extractor coupled to an output signal of the balanced low-pass filter;
   - an amplifier coupled to an output signal of the extractor;
   - a phase shifter coupled to the amplifier; and
   - a subtractor coupled to the balanced low-pass filter and the phase shifter;
   - wherein the distortion generated by the mixer is extracted by the even mode extractor and applied to the desired signal of the subtractor thereby suppressing distortion.

2. The apparatus of claim 1 wherein the balanced low-pass filter is comprised of a pair of pi filters.

3. The apparatus of claim 1 wherein the subtractor is comprised of a pair of evenly balanced resistors.

4. The apparatus of claim 1 wherein the even mode distortion extractor and the phase shifter are implemented as part of an operational amplifier.

5. A method for suppressing distortion in a direct conversion receiver comprising the following steps:
   - converting a balanced RF input signal into a balanced current signal;
   - mixing the current signal with an output signal of a local oscillator;
   - converting the mixed current and local oscillator signals into a voltage signal;
   - filtering the converted voltages signal;
   - extracting a distortion component of the voltage signal;
   - phase-shifting the distortion component of the voltage signal; and

subtracting the phase-shifted distortion component of the voltage signal from the filtered converted voltage signal.

6. The method of claim **5** wherein the distortion component of the voltage signal is an even-mode component.

7. The method of claim **5** wherein distortion component of the voltage signal is phase-shifted one hundred eighty degrees.

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